PSEUDO RANDOM OPTIMIZED BUILT-IN SELF-TEST

ABSTRACT

Test apparatus provides both flat pseudo random test patterns in combination with weighted pseudo random test patterns that the weight applied to every latch in the LSSD chain can be changed on every cycle. This apparatus fully integrates on-chip weighted pattern generation with either internal or external weight set selection. With WRP test technology, the WRP patterns are generated by the tester either externally or internally to the DUT and loaded via the shift register inputs (SRIs or WPIs) into the chip's shift register latches (SRLs). A test (or LSSD tester loop sequence) includes loading the SRLs in the SR chains with a WRP, pulsing the appropriate clocks, and unloading the responses captured in the SRLs into the multiple input signature register (MISR). Each test can then be applied multiple times for each weight set, with the weight-set assigning a weight factor or probability to each SRL. The weight factor is typically of binary granularity with probabilities of:

p{"1"} = [0,... 1/8, 1/4, 1/2, 3/4,7/8, ... or 1] for similarly for p{0}.

With the above arrangement, only specific subsets of SRLs of the LSSD chain need to be weighted with each weight-set. The remaining SRLs, those not included in the weighted subset, can be loaded with "flat" pseudo-random patterns generated by the built-in LFSR. Furthermore, multiple sets of weights and associated with multiple subsets of SRLs and also be used. From "none" to "all" the latches in the array can be modified on each scan shift cycle.